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EXAMINER	
YIGDALL, MICHAEL J	
ART UNIT	**PAPER NUMBER**
2122	9

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,813	SPRUNT ET AL.	
	Examiner	Art Unit	
	Michael J. Yigdall	2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2000 and 06 April 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5 and 6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-24 are pending and have been be examined. The date of priority considered for the application is 29 December 2000.

Information Disclosure Statement

2. The information disclosure statement filed on 6 April 2001 (Paper No. 5) cites U.S. Pat. No. 5,696,939 issued to Berc et al. However, the patent number and the name of the patentee do not correspond to the same document. U.S. Pat. No. 5,796,939 is perhaps the intended reference. Appropriate correction is required.

Claim Objections

3. Claim 23 is objected to because of the following informalities: The phrase "one more multiplexors" should likely be replaced with --one or more multiplexors--. Appropriate correction is required. The claim has been interpreted assuming this correction to be made.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-3, 10-12, 18-20 and 22-24 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Pat. No. 5,835,705 to Larsen et al.

With respect to claim 1, Larsen et al. disclose a computer system which includes an apparatus for monitoring the performance of a multithreaded processor (see the title and abstract), said apparatus comprising:

(a) a processor adapted to execute a plurality of threads simultaneously, each thread including a series of instructions (see column 3, lines 39-55, which shows a multithreaded processor and concurrent threads comprising groups of instructions);

(b) a plurality of programmable event counters to count two or more independent events generated by one or more threads of said plurality, said two or more events selected from a predetermined list of events resulting from the normal operation of said processor (see column 4, lines 50-57, which shows a plurality of programmable counters for recording events generated by processor components selected from a predetermined list);

(c) one or more registers to control the operation of said event counters, each register also selecting the events to be counted from said list of events (see column 5, lines 7-17, which shows control registers used to set the mode of operation and to select the events recorded by the counters); and

(d) an access location to allow access to said event counters to determine a current count of said events (see column 4, lines 57-61, which shows that the counter values are output to integer registers, i.e. access locations).

With respect to claim 2, Larsen et al. disclose the computer system of claim 1 wherein said access location allows access to determine said count without disturbing the operation of said counters (see column 7, lines 40-52, which shows accessing the registers to read a count without disturbing the operation of the counters).

With respect to claim 3, Larsen et al. disclose the computer system of claim 1 wherein each register comprises a first field of bits for choosing one or more events to be counted (see column 5, lines 7-17, which shows control registers having bit fields for selecting one or more events to be counted).

With respect to claim 10, Larsen et al. disclose an apparatus for monitoring the performance of a multithreaded processor (see the title and abstract) comprising:

(a) processing means for processing a plurality of threads simultaneously, each thread including a series of instructions (see the explanation for part (a) of claim 1 above);

(b) counting means for counting one or more events generated by one or more threads of said plurality, said one or more events selected from a predetermined list of events resulting from the normal operation of said processor (see the explanation for part (b) of claim 1 above);

(c) controlling means for controlling said counting means and for choosing said one or more events from said list (see the explanation for part (c) of claim 1 above); and

(d) accessing means for accessing said counting means to determine the count of said one or more events (see the explanation for part (d) of claim 1 above).

With respect to claim 11, see the explanation for part (b) of claim 1 above.

With respect to claim 12, see the explanation for part (c) of claim 1 and the explanation for claim 3 above.

With respect to claim 18, Larsen et al. disclose a method for monitoring the performance of a multithreaded processor (see the title and abstract), said method comprising:

(a) executing a plurality of threads simultaneously, each thread including a series of instructions (see the explanation for part (a) of claim 1 above);

(b) counting a plurality of independent events generated by one or more threads of said plurality, said plurality of events selected from a predetermined list of events resulting from the normal operation of said processor (see the explanation for part (b) of claim 1 above);

(c) controlling the operation of said event counters, each register also selecting the events to be counted from said list of events (see the explanation for part (c) of claim 1 above); and

(d) accessing said event counters to determine a current count of said events (see the explanation for part (d) of claim 1 above).

With respect to claim 19, see the explanation for claim 3 above.

With respect to claim 20, Larsen et al. disclose the method in claim 19 wherein said qualifying includes requiring that said plurality of events have a preselected thread ID (see column 6, lines 54-67, and column 7, lines 1-3, which show selecting and routing events based on the identity of the thread to which they correspond).

With respect to claim 22, Larsen et al. disclose an apparatus incorporated in an integrated circuit (IC) for monitoring the performance of a multithreaded central processing unit (CPU) by recording the occurrence of events resulting from the normal operation of said CPU (see the title and abstract; see also column 2, lines 55-61, which show that the apparatus is incorporated in an integrated circuit), each event comprising an electric signal representing the incidence of a particular activity within said IC (see column 5, lines 7-17, which shows the routing of event signals that are generated by components of the processor), said apparatus comprising:

(a) a processor adapted to execute a plurality of threads simultaneously, each thread including a series of instructions (see the explanation for part (a) of claim 1 above);

(b) first and second programmable counters operated synchronously to record first and second selected events respectively (see the explanation for part (b) of claim 1 above);

(c) logic circuitry to couple said first and second selected events to said first and second programmable counters, respectively (see Figs. 2 and 3);

(d) a control register coupled to said logic circuitry to select said first and second selected events (see the explanation for part (c) of claim 1 above); and

(e) an access location to allow access to said counters (see the explanation for part (d) of claim 1 above).

With respect to claim 23, Larsen et al. disclose the apparatus of claim 22 wherein said logic circuitry comprises one or more multiplexors coupled to receive a plurality of events (see item 82 of Fig. 2, and items 82a and 82b of Fig. 3).

With respect to claim 24, Larsen et al. disclose the apparatus of claim 23 wherein said logic circuitry is adapted to select said first and second selected events from said plurality of events according to their thread ID (see column 6, lines 54-67, and column 7, lines 1-3, which show selecting and routing events based on the identity of the thread to which they correspond; see also Fig. 3, which shows the logic circuitry).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 4, 5, 9, 13, 14 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Larsen et al. in view of U.S. Pat. No. 6,205,468 to Diepstraten et al.

With respect to claim 4, Larsen et al. disclose the computer system of claim 3, but do not show the limitation wherein each register further comprises a second field of bits for choosing one or more events to be masked and not counted.

Larsen et al. does show control registers with bit fields used to select events to be recorded, set the mode of operation, and to enable or disable event counting (see column 5, lines 7-17).

Diepstraten et al. disclose the limitation above in terms of an event masker associated with an event recorder (see column 4, lines 42-50, which shows event masking used to select one or more events to be ignored; see also item 90 of Fig. 3, which shows the control bits of the event mask register).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Larsen et al. with the feature of Diepstraten et al., for the purpose of reducing the number of events that will be processed (see Diepstraten et al., column 4, lines 42-50).

With respect to claim 5, Larsen et al. in view of Diepstraten et al. disclose the computer system of claim 4 wherein each register further comprises a third field of bits for choosing from which of said plurality of threads an event is to be counted according to each thread's ID (see Larsen et al., column 6, lines 54-67, and column 7, lines 1-3, which show choosing the thread for which an event is to be counted based on its identity).

With respect to claim 9, Larsen et al. in view of Diepstraten et al. disclose the computer system of claim 5 wherein said predetermined list of events includes hardware performance and breakpoint events (see Larsen et al., column 5, lines 46-56, which shows the list of events, including hardware performance events such as instructions completed and processor cycles, and breakpoint events such as thread switch counts).

With respect to claim 13, see the explanation for claim 4 above.

With respect to claim 14, see the explanation for claim 5 above.

With respect to claim 17, see the explanation for claim 9 above.

8. Claims 6-8, 15, 16 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Larsen et al. in view of Diepstraten et al. as applied to claims 4, 5, 9, 13, 14 and 17 above, and further in view of U.S. Pat. No. 5,657,253 to Dreyer et al.

With respect to claim 6, Larsen et al. in view of Diepstraten et al. disclose the computer system of claim 5, but do not show the limitation wherein said third field of bits can further choose from which of said plurality of threads an event is to be counted according to each thread's current privilege level (CPL).

Larsen et al. does show control registers with bit fields used to select events to be recorded, set the mode of operation, and to enable or disable event counting (see column 5, lines 7-17).

Dreyer et al. disclose the limitation above in a performance monitoring system (see column 4, lines 39-46, which shows a bit in a control register used to enable event counting based on the current privilege level).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Larsen et al. and Diepstraten et al. with the feature taught by Dreyer et al., for the purpose of differentiating events in terms of supervisor and application levels of operation (see Dreyer et al., column 4, lines 60-65).

With respect to claim 7, Larsen et al. in view of Diepstraten et al. disclose the computer system of claim 6, but do not show the limitation wherein said counters can be stopped and cleared before a new event is selected.

Larsen et al. does show that the counters are software-writable (see column 4, lines 50-57).

Dreyer et al. further disclose the limitation above in a performance monitoring system (see column 3, lines 19-22, which shows that the counters can be reset using an instruction).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Larsen et al. and Diepstraten et al. with the feature taught by Dreyer et al., for the purpose of clearing the counter values with software.

With respect to claim 8, Larsen et al. in view of Diepstraten et al. disclose the computer system of claim 7, but do not show the limitation wherein said counters can be preset to a certain state.

Larsen et al. does show that the counters are software-writable (see column 4, lines 50-57).

Dreyer et al. further disclose the limitation above in a performance monitoring system (see column 3, lines 19-22, which shows that the counters can be preset to a certain value).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Larsen et al. and Diepstraten et al. with the feature taught by Dreyer et al., for the purpose of presetting the counters to enable functions such as countdowns (see Dreyer et al., column 4, lines 21-30).

With respect to claim 15, see the explanation for claim 6 above.

With respect to claim 16, Larsen et al. in view of Diepstraten et al. disclose the apparatus of claim 15 wherein said accessing means comprise instruction means within said processor for reading a count from each of said counters (see Larsen et al., column 7, lines 40-52, which shows receiving an instruction used to read a counter).

With respect to claim 21, see the explanation for claim 6 above.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S. Pat. No. 6,256,775 to Flynn discloses a performance monitor for recording events in a multithreaded processor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Yigdall whose telephone number is (703) 305-0352. The examiner can normally be reached on Monday through Friday from 8:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (703) 305-4552. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

MY

Michael J. Yigdall
Examiner
Art Unit 2122

mjy
October 20, 2003

JOHN CHAVIS
PATENT EXAMINER
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